Remarks

Claims 1-20 remain in this application. Claims 1-20 have been amended. Claims 1, 2, 12 and 18 are independent claims.

A. Formalities

Applicants have amended errors in the specification and the detailed drawings (Fig. 6). The amended sentences and drawing are consistent with the specification as originally filed and consistent with the amended claims. No new matter has been added.

B. Allowable Subject Matter

Applicants note with appreciation that in the Office action dated March 18, 2005, it was noted that claims 1-20 are patentable over the prior art. Thus, the claims would be allowed if rejections under 35 U.S.C. 112, second paragraph, and 35 U.S.C. 101 are overcome.

C. Errors Found in Specification

The disclosure was objected to due to errors in paragraphs [0037] and [0050].

1. Line 7 of paragraph [0037], as originally filed, reads "there may be am error tolerance adjustment." The line has been amended to read "there may be an error tolerance adjustment."

2. Line 9 of paragraph [0050] describes "a sufficient time interval (i.e., T_{hold})". The line has been amended to describe "a sufficient time interval 148 (i.e., T_{hold})".

3. Additional amendments to paragraph [0050], line 7 have been made. These amendments were made to be consistent with the amended drawing, Fig. 6. Line 7, as originally filed, describes a "clock edge 20 of the tester cycle 18 (Fig. 2A)". The amended line 7 describes a "clock edge 149 of the tester cycle".

Amendments to the Drawings:

In Fig. 6, delete the reference numeral "18" and its associated tagline.

In Fig. 6, delete the reference numeral "20" and insert in place thereof the reference numeral - -149- -.

Entry of the proposed amendments to the drawings is respectfully requested. No new matter has been added.

D. Patentability of Claims 2-11 under 35 U.S.C. 112

Claims 2-11 were rejected under 35 U.S.C. 112 for failing to particularly point out and distinguish the subject matter of the invention. Specifically, in claim 2, the limitation "said synchronous short-delay sequence" was deemed to have insufficient antecedent basis. In response, Applicants have amended claim 2 to include the feature of generating a synchronous short-delay sequence by successively repeating a first delay-adjusted clock period having a state which is delayed by the first overlapping time interval.

Support for the amendment resides on page 13, paragraph [0045], wherein the clock period having the overlapping cycle 102 is duplicated in every base period 100. The duplicating step provides a synchronous short-delay sequence 106 of Fig. 4, where the overlapping cycle is repeated in every base period at the identical time location. Applicants respectfully assert claim 2, as amended, provides a proper antecedent basis for all limitations of the claim and satisfies the requirements of 35 U.S.C. 112, second paragraph. Reconsideration is requested.

E. Office Action Recommendations

For purposes of clarification, the Examiner made suggestions to Applicants' claims. All suggestions have been incorporated into the amended claims. The amended portions of the claims appear below.

Claim 2 (lines 26-27 of amended claim): "said particular IC" has been replaced by "said particular IC design".

Claim 6 (line 3): "said IC" has been replaced by "said IC design".

Claim 12 (lines 19-20 of amended claim): "said first state time interval" has been replaced by "said first state overlapping time interval".

Claim 19 (line 3): "said IC" has been replaced by "said simulated IC".

F. Patentability of Claims 1, 2, 12 and 18 under 35 U.S.C. 101

Claims 1-20 were rejected under 35 U.S.C. 101 for allegedly being directed to the manipulation of abstract ideas not tangibly embodied,

not being in the technological arts and not providing a useful or tangible result. In response, Applicants have amended claims 1-20 to conform to a Beauregard claim format.

Claim 1 was amended to describe the invention as a computer-readable storage medium having a stored computer-executable instruction set for initiating a method for driving the simulation testing of a design of an integrated circuit. The invention of the amended claim is tangibly embodied within the storage medium. It is known to those of ordinary skill in the art that the verification of the operation of a prototype (page 2, paragraph [0002]) design prior to fabrication ensures that the requirements defined by the chip specifications are satisfied. The verification process provides feedback to engineers so that any detected defects can be corrected. This is potentially significant, since eliminating problems at an early stage results in substantial savings in the time and cost of manufacturing. Applicants respectfully assert that the invention has a practical use for establishing a successful test simulation.

Claim 2 was amended to describe the invention as a computer-readable storage medium having computer-executable program code configured to implement a method of generating a synchronous sequence of test vectors from information originating within an asynchronous environment. Applicants' invention is tangibly embodied within the medium. The computer-executable program code configured to implement the method of the invention would cause a computer executing the program code to implement the method steps of the invention. A tangible use for the invention resides in the last sub-paragraph of the claim (line 36), in which the synchronous short-delay sequence is compared with timing of the states of the synchronous long-delay sequence to generate the synchronous sequence of test vectors, including time aligning said synchronous short-delay and long-delay sequences to detect a plurality of overlapping time intervals for locating the synchronous sequence of test vectors.

Claim 12 has been amended to describe the system as a computer-readable medium having executable instructions for driving a test vector generator for generating a synchronous sequence of test vectors. An article of manufacture (computer-readable medium) has executable instructions to drive a test vector generator. The test vector generator and the instructions are cooperative to comprise a simulation module, delay module, overlaying module, duplication module and a sequence overlaying module.

The simulation module is described as being enabled to generate a simulation synchronous sequence of states under a system simulation environment. The simulation synchronous sequence includes a plurality of timing regions for identifying operations of an integrated circuit design. As previously remarked, the usefulness of subjecting the design of an integrated circuit to a simulated test environment to identify design errors is known in the art. Early detection of design errors results in both cost and time savings.

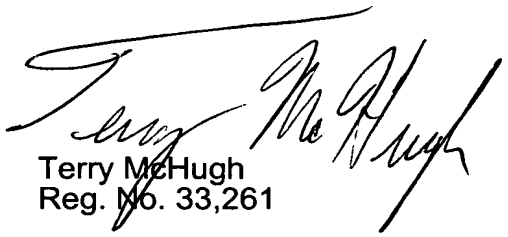
Claim 18 was amended to describe a program storage device having computer-executable code for implementing a method for converting asynchronous states into synchronous states to generate a synchronous sequence of test vectors for verifying functionality of a simulated integrated circuit design. The executable code is tangibly embodied in a program storage device readable by a computer to execute the method described in the claim.

Applicants respectfully assert that the claim as amended presents a tangible result in that by performing each of the steps of the method, a capability of verifying the functionality of a simulated integrated storage device is enabled.

It is therefore submitted that all the amended independent claims 1, 2, 12 and 18 are tangibly embodied and in the technological arts. In addition, each has a practical use and tangible result.

Applicants respectfully request reconsideration of the claims in view of the amendments and remarks made herein. A notice of allowance is earnestly solicited. In the case that any issues regarding this application can be resolved expeditiously via a telephone conversation, Applicants invite the Examiner to call Terry McHugh at (650) 969-8458.

Respectfully submitted,
Robert C. Aitken et al.



Date: May 10, 2005

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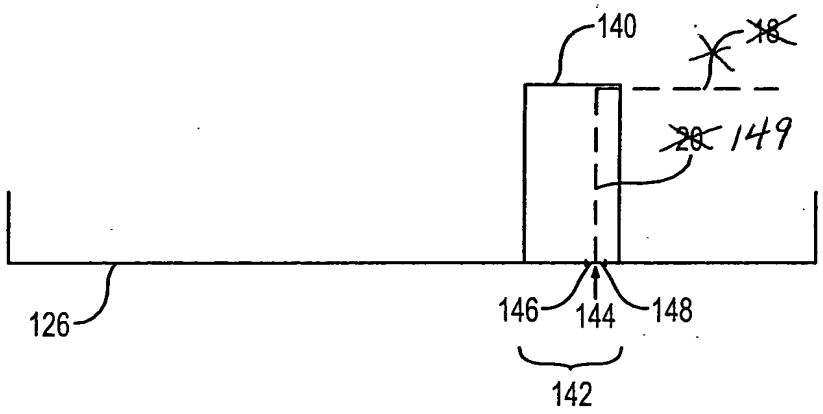

FIG. 6